What is claimed is:

1. A computer system for fetching, decoding and executing instructions comprising:

storage circuitry for holding a plurality of instructions at respective storage locations, said plurality of instructions being arranged in instruction strings, each string comprising a first instruction and a set of subsequent instructions;

instruction fetch circuitry for fetching a sequence of instructions from said storage circuitry and including an indicator for providing an indication of a next address at which a next fetch operation is to be effected;

execution circuitry for executing fetched instructions, wherein at least some of said instruction strings each includes a set branch instruction (SET) which provides an indication of a target location from which a subsequent instruction may be fetched, the subsequent instruction being from a different instruction string, and wherein said instruction fetch circuitry is operated responsive to execution of a said set branch instruction (SET) to fetch in parallel subsequent instructions from said string containing said set branch instruction and new instructions from said different instruction string commencing from said target location while said subsequent instructions continue to be executed;

a target store for holding the indication of said target location, said indication being loaded into said store on execution of said set branch instruction (SET) and being held in said store as a valid indication until execution of a subsequent set branch instruction; and

select circuitry responsive to generation of an effect branch (DO) signal indicative that further instructions to be executed are said new instructions, to cause said execution circuitry to execute said new instructions and to cause said instruction fetch circuitry to fetch again new instructions commencing from said target location.

2. A computer system according to claim 1 wherein said instruction fetch circuitry comprises two instruction buffers, a first buffer for holding subsequent instructions connected to said execution circuitry, and a second buffer for holding new instructions wherein the contents of said second buffer are copied into said first buffer responsive to generation of said effect branch (DO) signal.

3. A computer system according to claim 1 wherein said instruction fetch circuitry includes two instruction fetchers for fetching respectively said subsequent instructions and said new instructions and wherein said select circuitry is operable to connect a selected one of said instruction fetchers to said execution circuitry.

4. A computer system according to claim 3 wherein said instruction fetch circuitry comprises a third instruction fetcher for fetching instructions to implement predicted conditional instructions.

5. A computer system according to claim 1 which includes a first register for holding an indication of the address from which a next instruction is to be fetched.

6. A computer system according to claim 1 wherein the target store holds the address from which the first instruction of a string of new instructions is to be fetched.

7. A computer system according to claim 1 wherein the set branch instruction identifies a special register which holds the address from which the first instruction of a string of new instructions is to be fetched.

8. A computer system according to claim 1 wherein the target store holds the address of a memory location which holds the address of the first instruction of a string of new instructions is to be fetched.

9. A computer system according to claim 1 which comprises decode circuitry for decoding said fetched instructions, said instruction fetch circuitry, decode circuitry and execution circuitry being arranged in a pipeline.

10. A computer system according to claim 1 wherein said at least one instruction string includes a further instruction which determines the branch point after which new instructions are to be executed, identification of said branch point causing generation of said effect branch signal to said select circuitry.

11. A computer system according to claim 10 wherein said further instruction is located at the branch point after which said new instructions are to be executed.

12. A computer system according to claim 10 wherein said further instruction is located in the string prior to the branch point after which further instructions to be executed are said new instructions, said further instruction indicating the branch point and wherein the computer system comprises a branch point register for holding said branch point.

13. A computer system according to claim 10 wherein said further instruction is a different instruction from said set branch instruction.

14. A computer system according to claim 13 wherein said further instruction defines a condition and determines that further instructions to be executed are new instructions only if that condition is satisfied.

15. A computer system according to claim 5 wherein said set branch instruction identifies the branch point after which further instructions to be executed are new instructions, said computer system comprising a branch point register for storing

said branch point and compare circuitry for generating said effect branch signal to the select circuitry when said branch point matches the address indicated by the first register.

16. A computer system according to claim 10 which comprises a return register for holding a return address being the address of the next instruction after said branch point, wherein said further instruction is effective to generate said effect branch signal and to save said return address in said return register and wherein said branch instruction identifies said return register to indicate the target location.

17. A method of operating a computer to fetch decode and execute instructions which computer has storage circuitry holding a plurality of instructions at respective storage locations, said plurality of instructions being arranged in instruction strings, each string comprising a first instruction and a set of subsequent instructions the method comprising:

fetching a sequence of instructions from said storage circuitry and providing an indication of a next address at which a next fetch operation is to be effected;

decoding said instructions;

executing each instruction in turn, wherein at least some of said instruction strings each include a set branch instruction (SET) which provides an indication of a target location from which a subsequent instruction may be fetched, the subsequent instruction being from a different instruction string;

on execution of said set branch instruction, holding the indication of said target location in a target store as a valid indication until execution of a subsequent set branch instruction, fetching in parallel subsequent instructions from the string containing said branch instruction and new

instructions from said different instruction string commencing from said target location;

continuing to execute said subsequent instructions until an effect branch signal is generated which indicates that further instructions to be executed are said new instructions; and

responding to said effect branch signal by commencing execution of said new instructions and fetching again new instructions commencing from said target location.

18. A method according to claim 17 wherein said subsequent instructions are held in a first buffer and said new instructions are held in a second buffer and wherein said effect branch signal causes the contents of said second buffer to be copied into said first buffer.

19. A method according to claim 17 wherein a first instruction fetcher fetches said subsequent instructions and a second instruction fetcher fetches said new instructions, said effect branch signal selecting which of said first and second instruction fetchers supplies instructions for execution.

20. A method according to claim 17 wherein the effect branch signal is generated responsive to execution of a further instruction which determines the branch point after which new instructions are to be executed.

21. A method according to claim 20 wherein said further instruction defines a condition and determines that further instructions to be executed are new instructions only if that condition is satisfied.

22. A method according to claim 17 wherein said branch instruction identifies the branch point after which further instructions to be executed are new instructions and

wherein said effect branch signal is generated when said branch point matches the address from which a next instruction is to be fetched.

23. A method according to claim 17 wherein the set branch instruction identifies as the target location the address from which the first instruction of a string of new instructions is to be fetched.

24. A method according to claim 17 wherein the set branch instruction identifies a special register which holds the target location.

25. A method according to claim 17 wherein the set branch instruction identifies the address of a memory location holding the target location.

26. A method according to claim 20 wherein execution of said further instruction causes a return address to be saved in a return register and wherein said branch instruction identifies the return register to indicate the target location.

27. A computer system for fetching, decoding and executing instructions comprising:

storage circuitry for holding a plurality of instructions at respective storage locations, said plurality of instructions being arranged in instruction strings, each string comprising a first instruction and a set of subsequent instructions;

instruction fetch circuitry for fetching a sequence of instructions from said storage circuitry and including an indicator for providing an indication of a next address at which a next fetch operation is to be effected;

execution circuitry for executing fetched instructions, wherein at least one of said instruction strings includes a set branch instruction (SET) which provides an indication of a target location from which a subsequent instruction may be

fetched, the subsequent instruction being from a different instruction string, and an effect branch instruction different from said set branch instruction and located at the branch point after which said new instructions are to be executed, and wherein said instruction fetch circuitry is operated responsive to execution of a said set branch instruction (SET) to fetch in parallel subsequent instructions from said string containing said set branch instruction and new instructions from said different instruction string commencing from said target location while said subsequent instructions continue to be executed; and

select circuitry responsive to execution of an effect branch (DO) instruction to cause said execution circuitry to execute said new instructions if a condition determined by the effect branch instruction is satisfied.

28. A computer system according to claim 27 wherein said instruction fetch circuitry comprises two instruction buffers, a first buffer for holding subsequent instructions connected to said execution circuitry, and a second buffer for holding new instructions wherein the contents of said second buffer are copied into said first buffer responsive to generation of said effect branch (DO) signal.

29. A computer system according to claim 27 wherein said instruction fetch circuitry includes two instruction fetchers for fetching respectively said subsequent instructions and said new instructions and wherein said select circuitry is operable to connect a selected one of said instruction fetchers to said execution circuitry.

30. A computer system according to claim 27 which includes a first register for holding an indication of the address from which a next instruction is to be fetched.

31. A computer system according to claim 27 which comprises a target register for holding an indication of the target location identified by the set branch instruction.

32. A computer system according to claim 31 wherein the target register holds the address from which the first instruction of a string of new instructions is to be fetched.

33. A computer system according to claim 31 wherein the set branch instruction identifies a special register which holds the address from which the first instruction of a string of new instructions is to be fetched.

34. A computer system according to claim 31 wherein the target register holds the address of a memory location which holds the address of the first instruction of a string of new instructions is to be fetched.

35. A computer system according to claim 27 which comprises decode circuitry for decoding said fetched instructions, said instruction fetch circuitry, decode circuitry and execution circuitry being arranged in a pipeline.

36. A computer system according to claim 27 which comprises a return register for holding a return address being the address of the next instruction after said branch point, wherein said further instruction is effective to generate said effect branch signal and to save said return address in said return register and wherein said branch instruction identifies said return register to indicate the target location.

37. A method of operating a computer to fetch decode and execute instructions which computer has storage circuitry holding a plurality of instructions at respective storage locations, said plurality of instructions being arranged in instruction strings, each string comprising a first

instruction and a set of subsequent instructions the method comprising:

fetching a sequence of instructions from said storage circuitry and providing an indication of a next address at which a next fetch operation is to be effected;

decoding said instructions;

executing each instruction in turn, wherein at least one of said instruction strings includes a set branch instruction (SET) which provides an indication of a target location from which a subsequent instruction may be fetched, the subsequent instruction being from a different instruction string;

on execution of said set branch instruction, fetching in parallel subsequent instructions from the string containing said branch instruction and new instructions from said different instruction string commencing from said target location;

continuing to execute said subsequent instructions until an effect branch instruction is executed which is located at the branch point after which new instructions are to be executed and which indicates that further instructions to be executed are said new instructions if a condition determined by the effect branch instruction is satisfied; and

responding to said effect branch signal by commencing execution of said new instructions.